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(54) ORGANIC LIGHT EMITTING DISPLAY HAVING ORGANIC LIGHT EMITTING DIODE CIRCUIT WITH VOLTAGE COMPENSATION AND TECHNIQUE THEREOF

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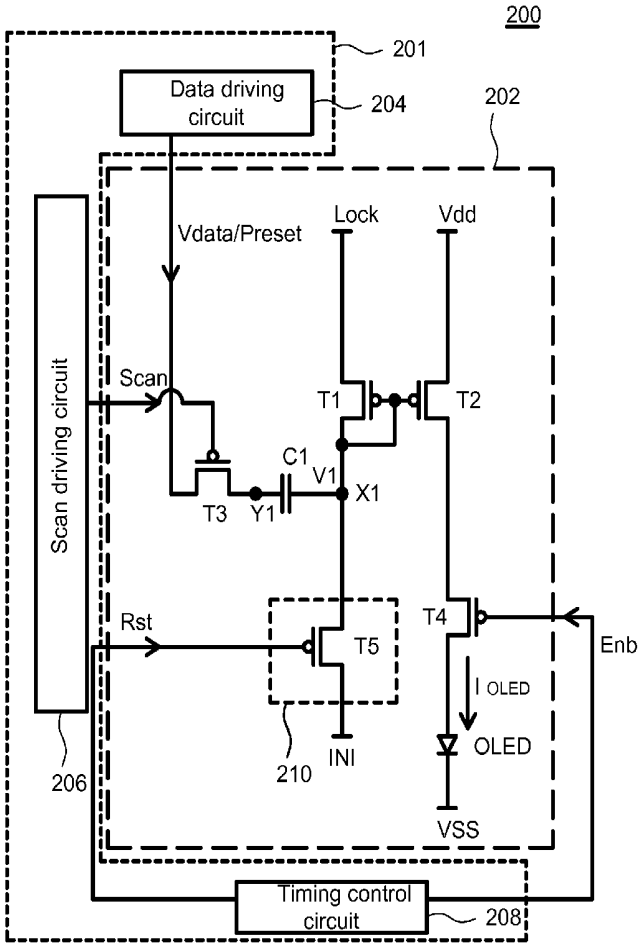
(57) **ABSTRACT**

An organic light emitting diode circuit of an organic light emitting display with voltage compensation technique includes a first capacitor, a first TFT, a second TFT, a third TFT, a reset circuit and an OLED. The first TFT has a first terminal for receiving a first voltage, and a second terminal coupled to its gate and a first end of the first capacitor. The second TFT has a first terminal for receiving a second reference voltage and a gate coupled to the gate of the first TFT. The third TFT is coupled to the first capacitor and receives a pixel voltage and scan signal. The reset circuit sets the first end of the first capacitor to have a first voltage level. The OLED has an anode coupled to a second terminal of the second TFT and a cathode for receiving a third reference voltage. The first voltage level is smaller than a voltage level of the first reference voltage.



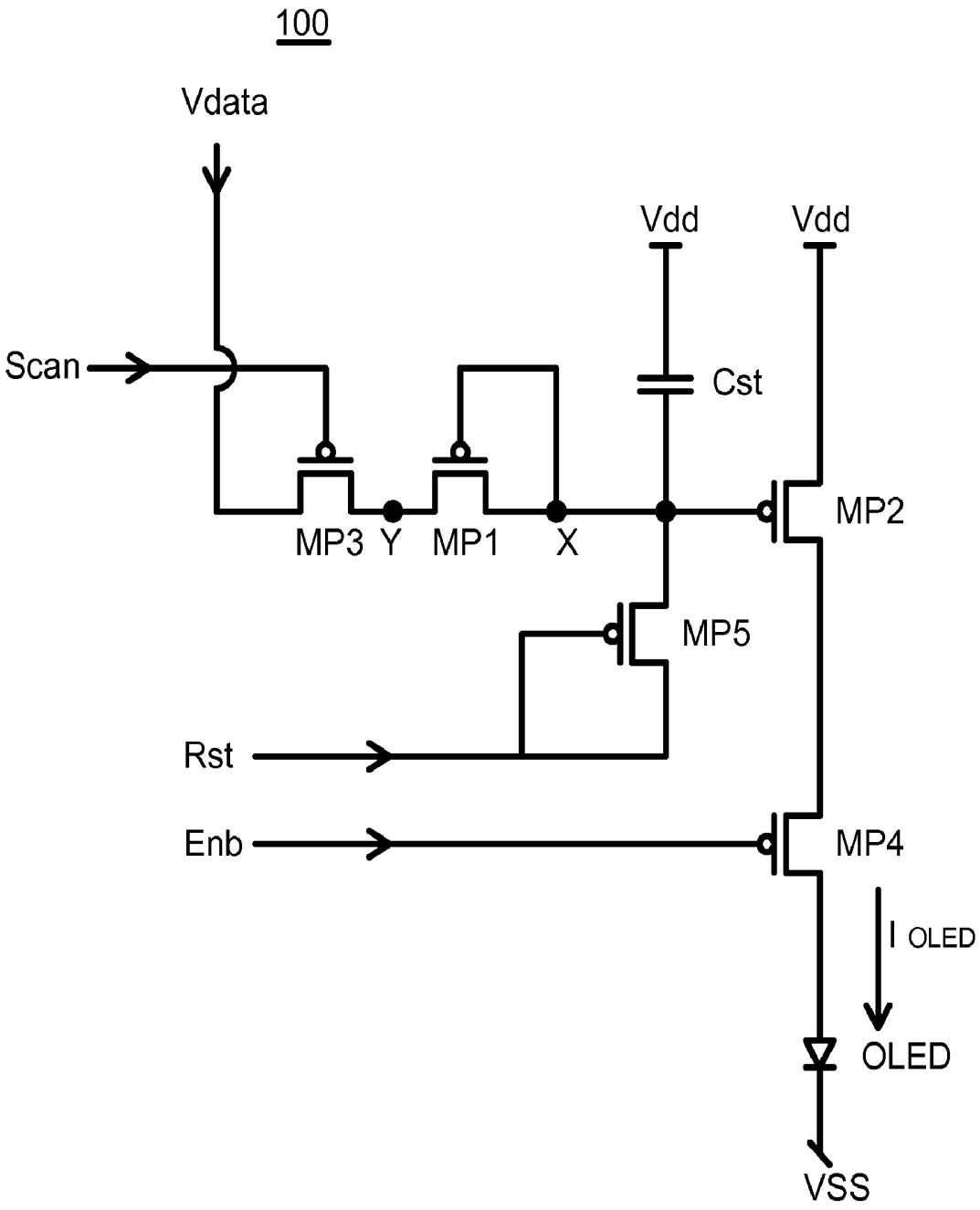


FIG. 1(PRIOR ART)

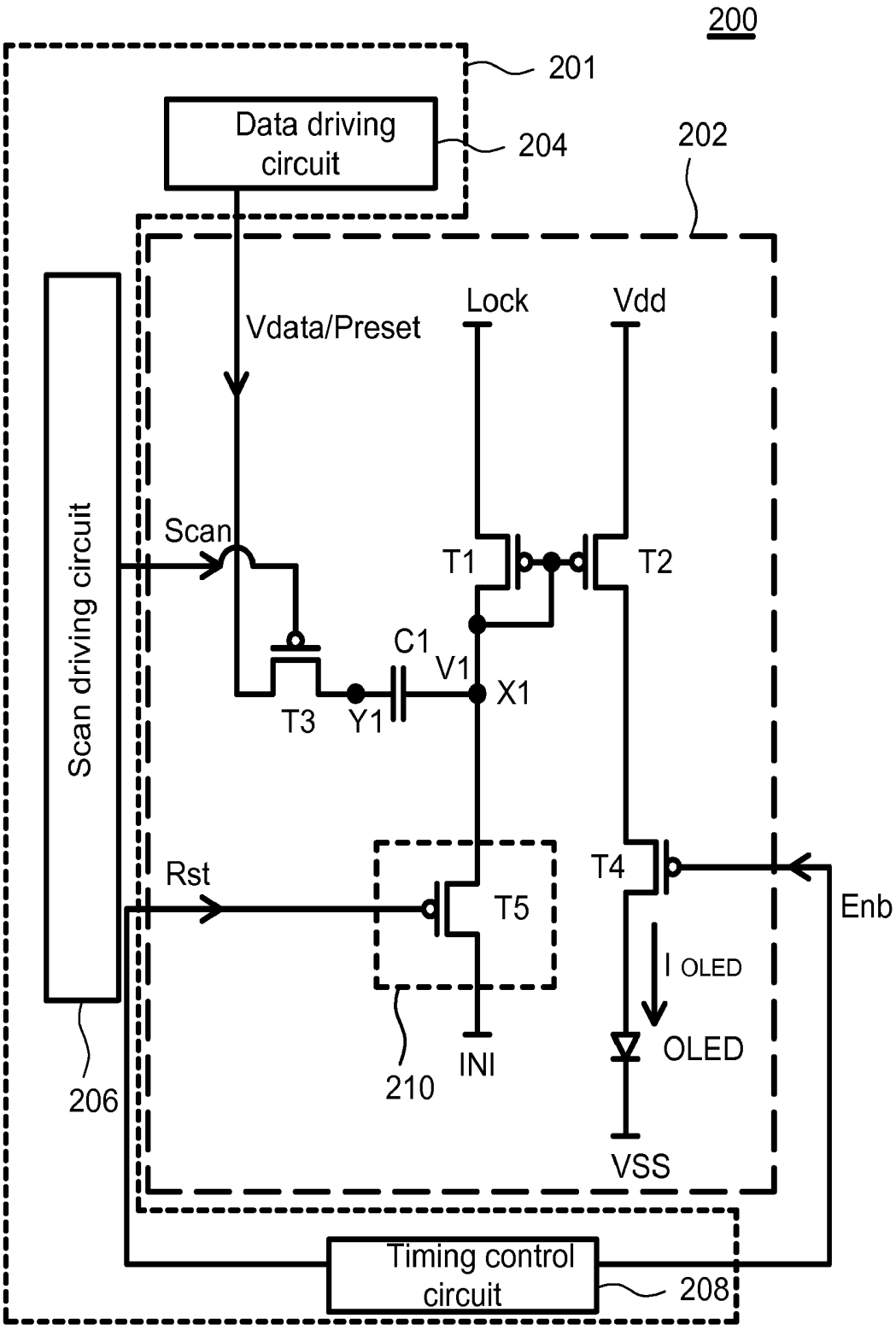

200
201
Data driving circuit
204
202
Vdata/Preset
Lock
Vdd
Scan driving circuit
Scan
T1
T2
C1
V1
X1
T3
Y1
Rst
T5
T4
Enb
I OLED
OLED
INI
210
206
VSS
Timing control circuit
208

FIG. 2

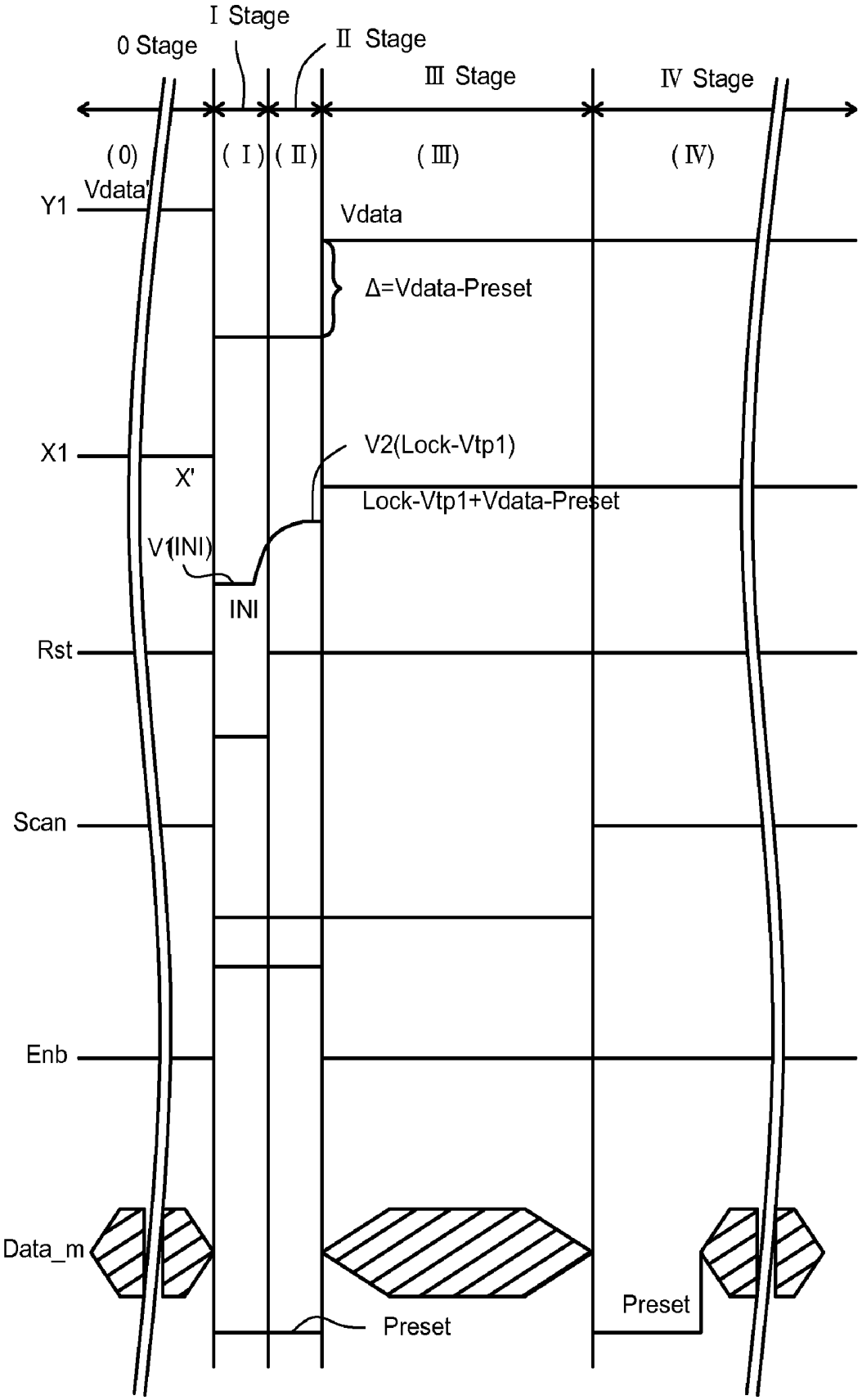

I Stage
0 Stage
II Stage
III Stage
IV Stage
(0)
(I)
(II)
(III)
(IV)
Y1
Vdata'
Vdata
Δ=Vdata-Preset
X1
X'
V2(Lock-Vtp1)
Lock-Vtp1+Vdata-Preset
V1(INI)
INI
Rst
Scan
Enb
Data_m
Preset
Preset

FIG. 3

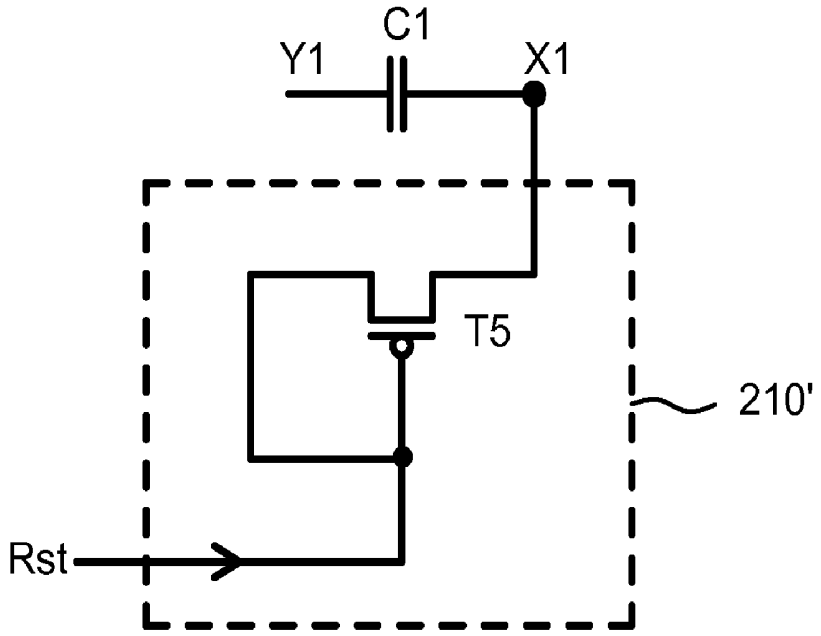


FIG. 4

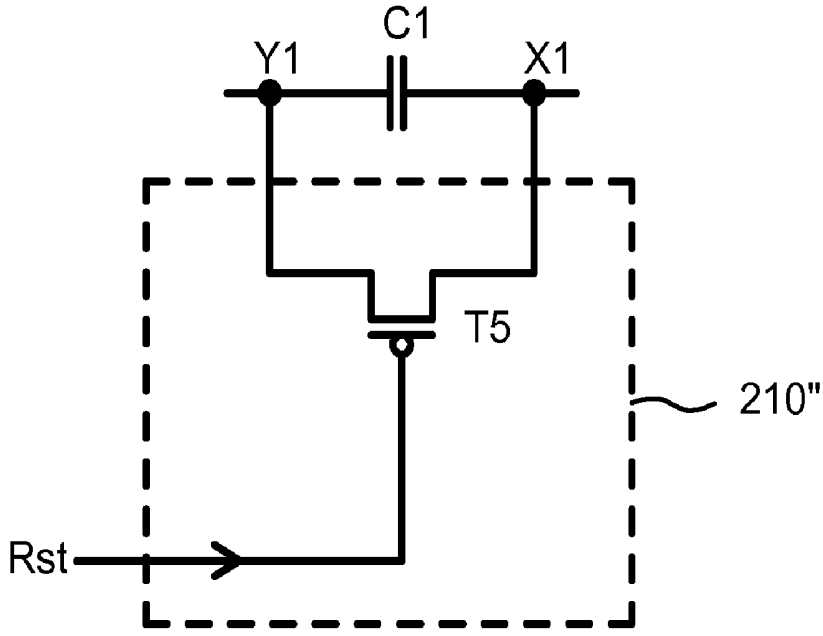


FIG. 5

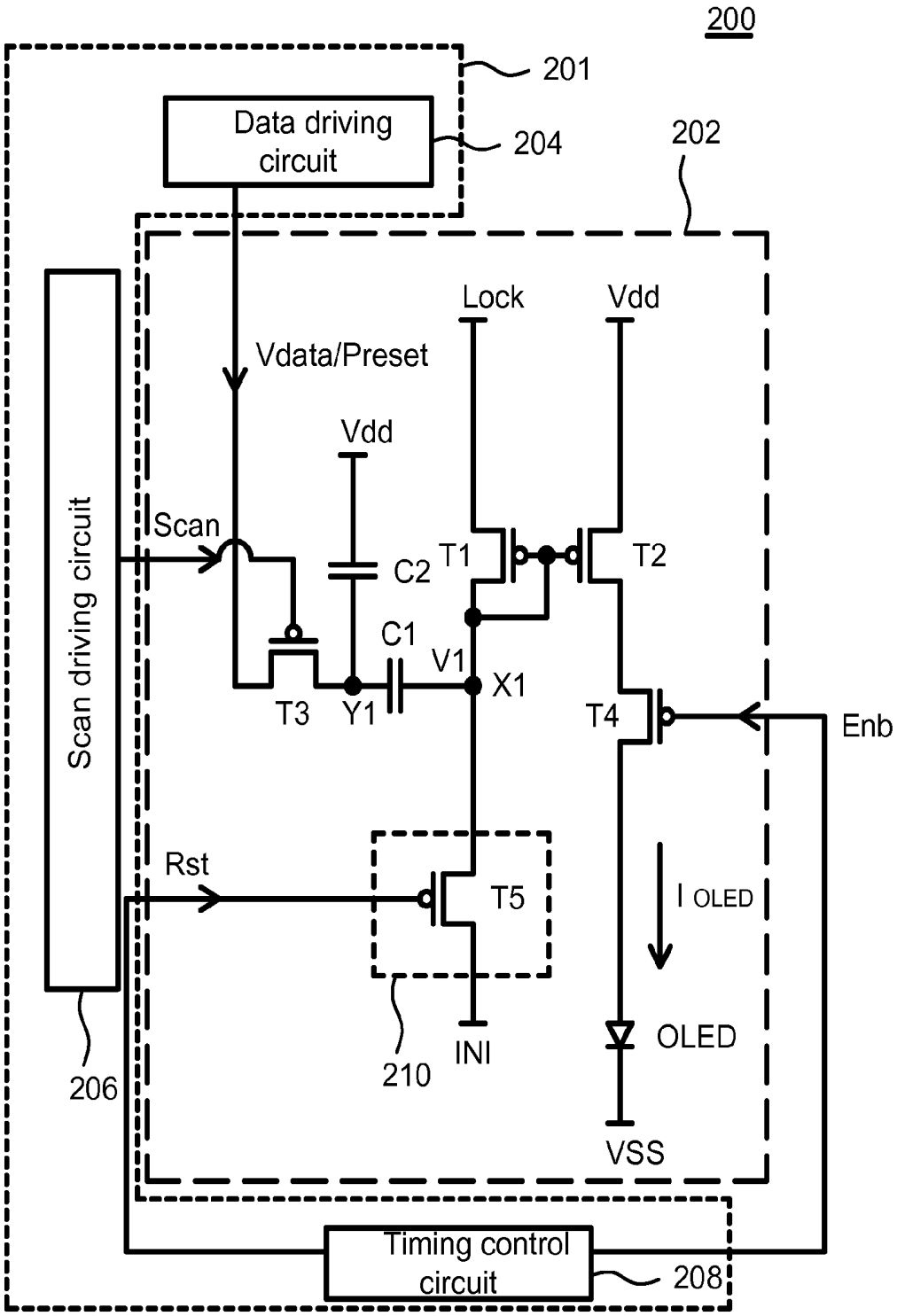

200
201
Data driving circuit
204
202
Lock
Vdd
Vdata/Preset
Vdd
Scan
C2
T1
T2
C1
V1
X1
T3
Y1
T4
Enb
Scan driving circuit
Rst
T5
I OLED
OLED
206
210
INI
VSS
Timing control circuit
208

FIG. 6

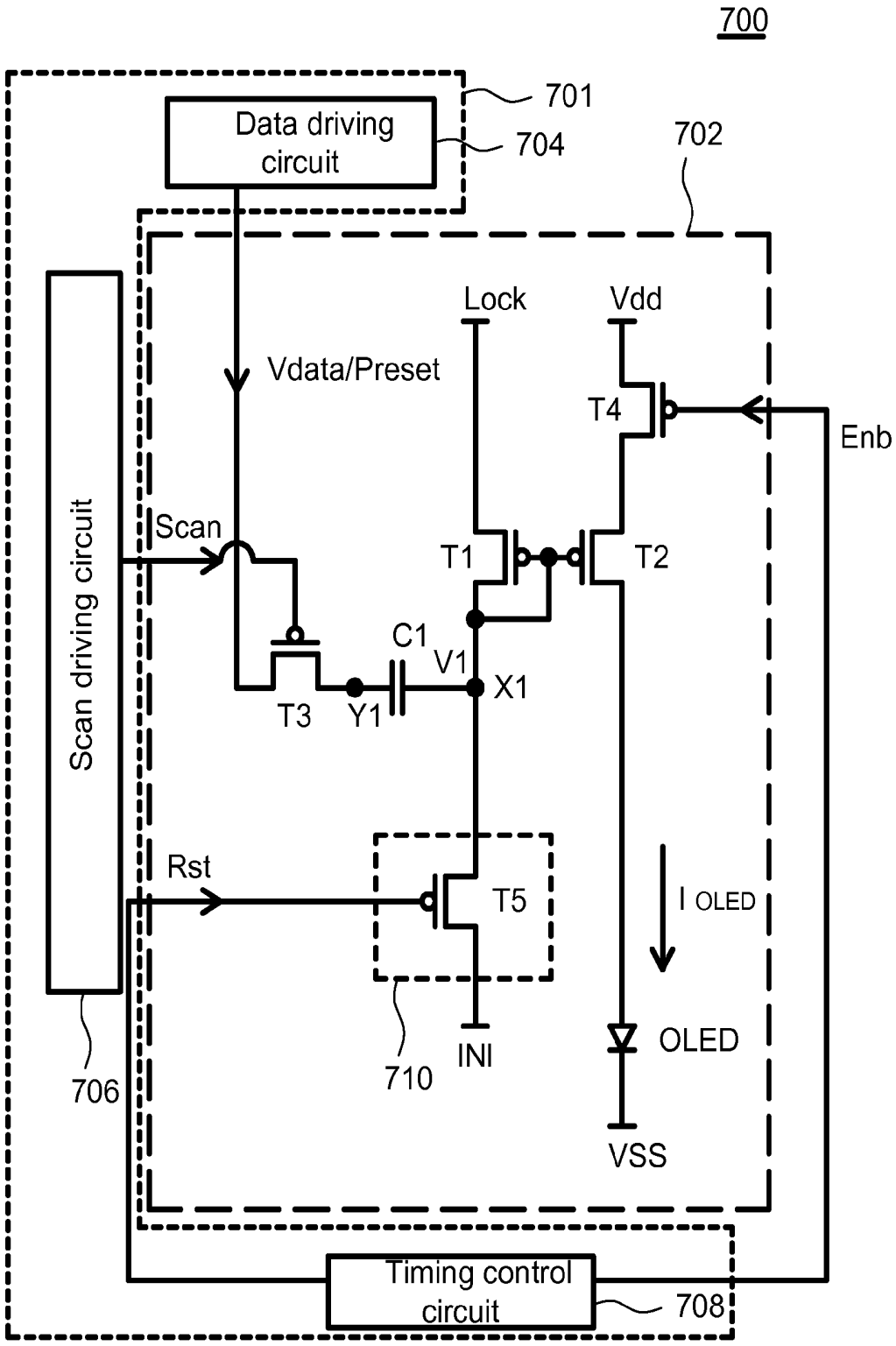

700
701
Data driving circuit
704
702
Lock
Vdd
Vdata/Preset
T4
Enb
Scan driving circuit
Scan
T1
T2
C1
V1
X1
T3
Y1
Rst
T5
I OLED
OLED
INI
710
706
VSS
Timing control circuit
708

FIG. 7

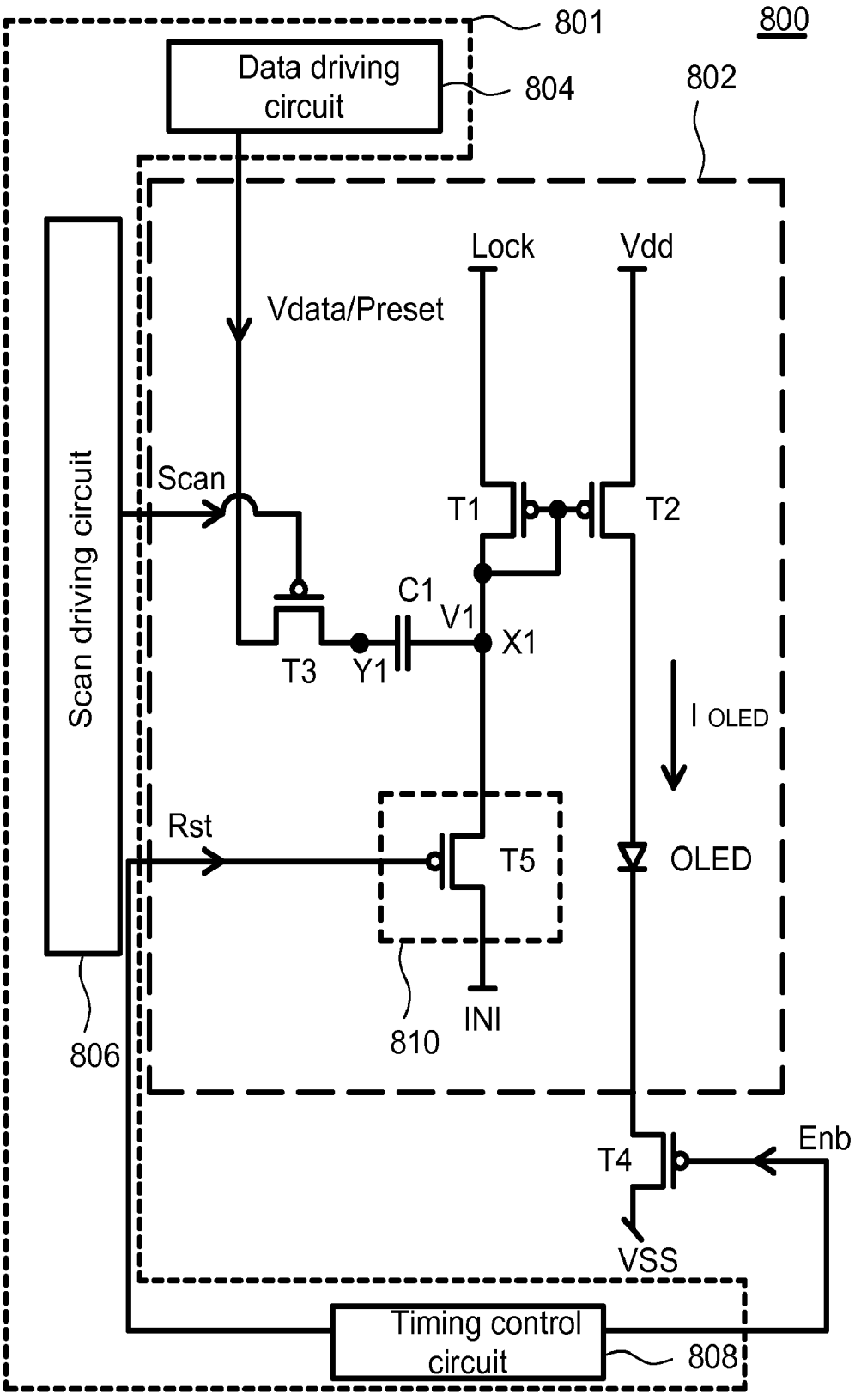

801
800
Data driving circuit
804
802
Lock
Vdd
Vdata/Preset
Scan driving circuit
Scan
T1
T2
C1
V1
X1
T3
Y1
I OLED
Rst
T5
OLED
806
810
INI
Enb
T4
VSS
Timing control circuit
808

FIG. 8

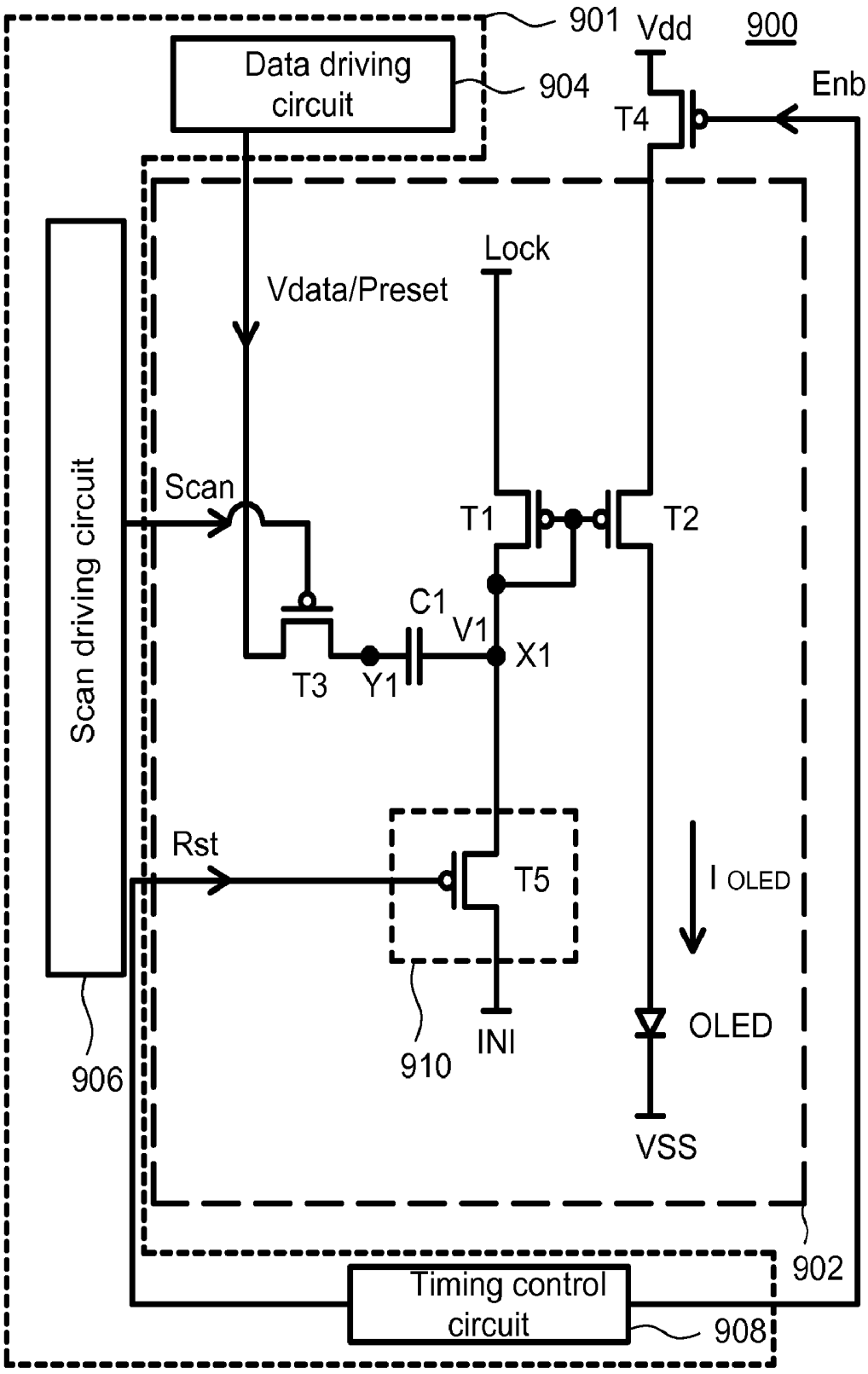

901
Vdd
900
Data driving circuit
904
Enb
T4
Lock
Vdata/Preset
Scan driving circuit
Scan
T1
T2
C1
V1
X1
T3
Y1
Rst
T5
I OLED
OLED
906
910
INI
VSS
902
Timing control circuit
908

FIG. 9

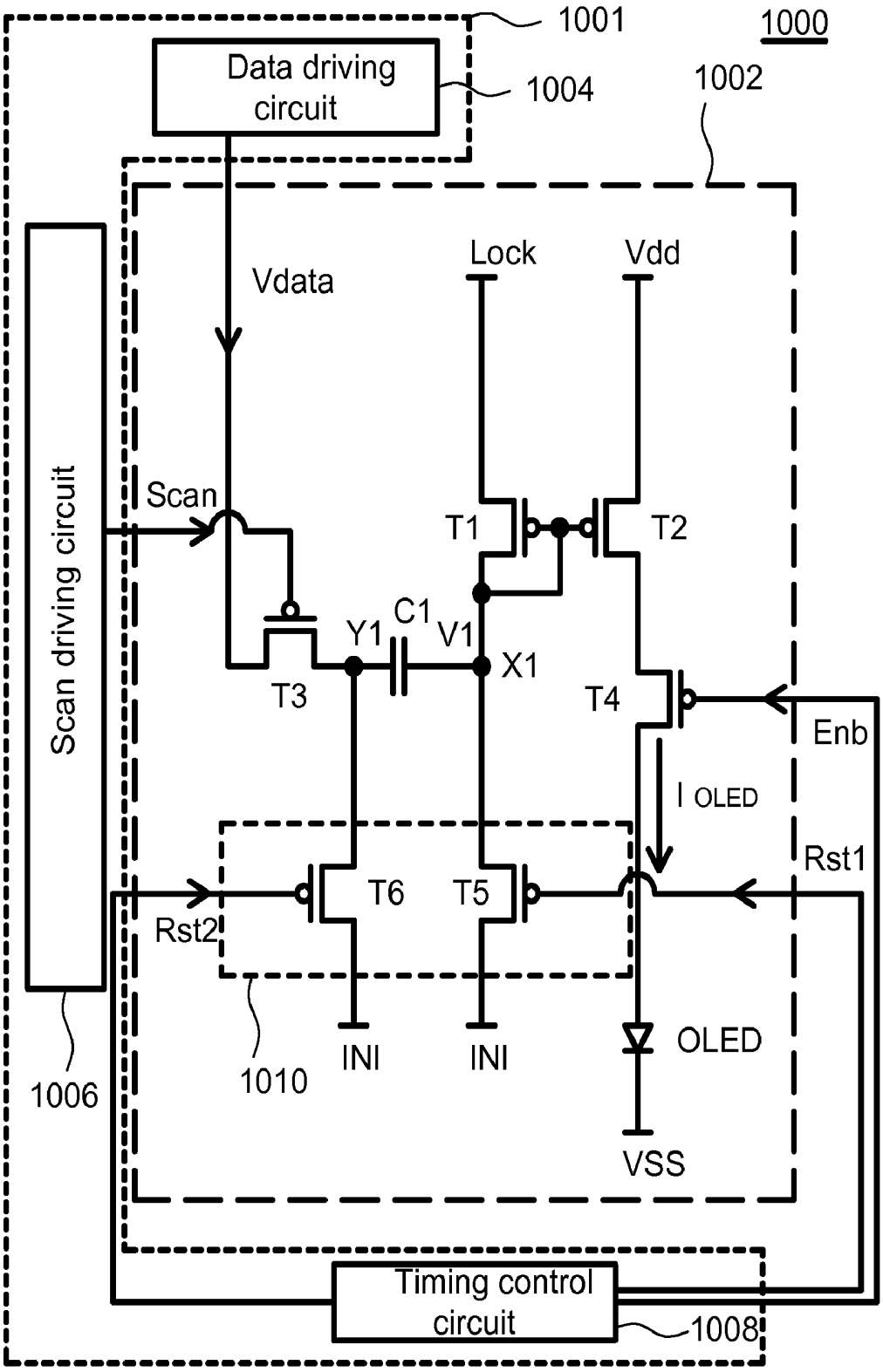

1001
1000
Data driving circuit
1004
1002
Vdata
Lock
Vdd
Scan driving circuit
Scan
T1
T2
C1
Y1
V1
X1
T3
T4
Enb
I OLED
Rst1
T6
T5
Rst2
INI
INI
OLED
1006
1010
VSS
Timing control circuit
1008

FIG. 10

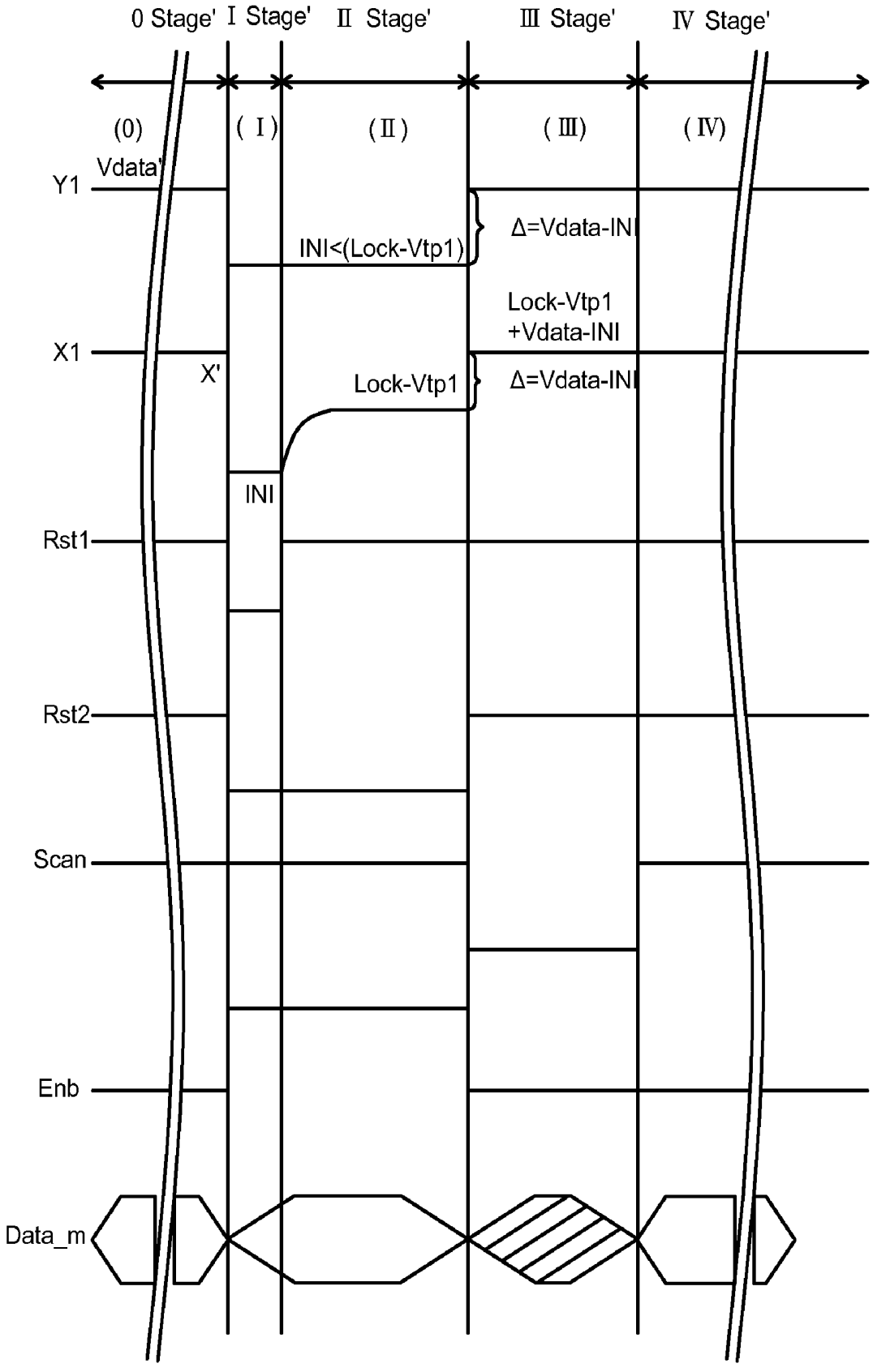

0 Stage'
I Stage'
II Stage'
III Stage'
IV Stage'
(0)
(I)
(II)
(III)
(IV)
Vdata'
Y1
X1
X'
INI<(Lock-Vtp1)
Δ=Vdata-INI
Lock-Vtp1
+Vdata-INI
Lock-Vtp1
Δ=Vdata-INI
INI
Rst1
Rst2
Scan
Enb
Data_m

FIG. 11

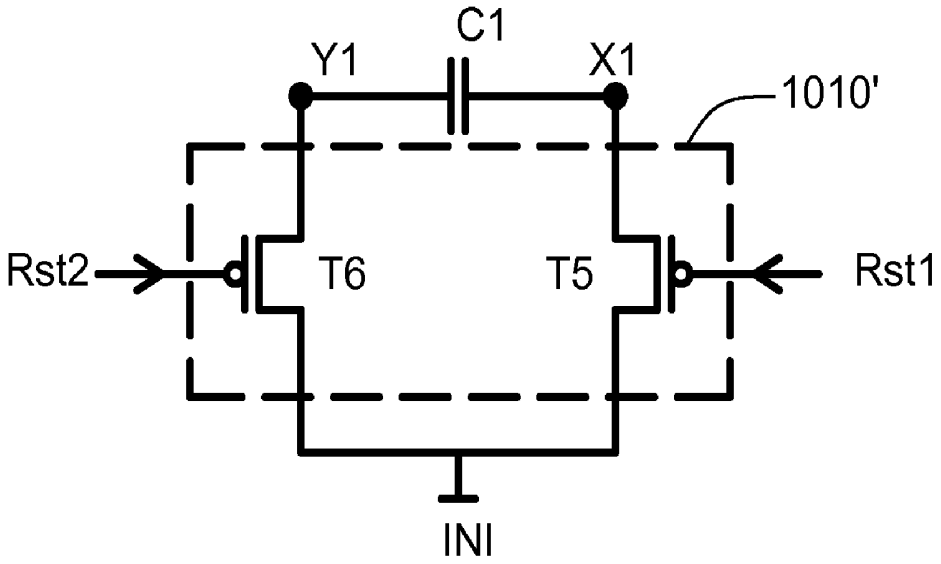


FIG. 12

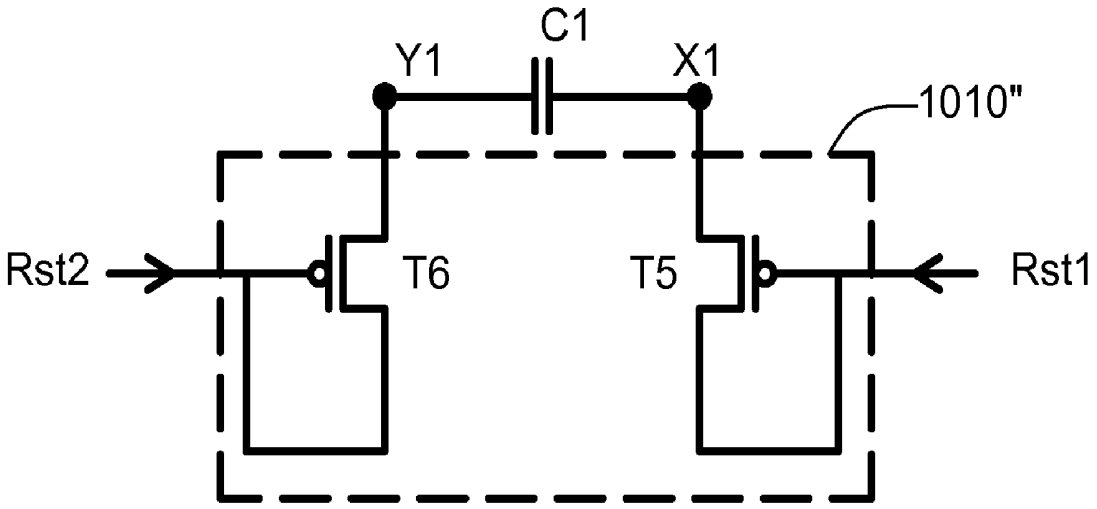


FIG. 13

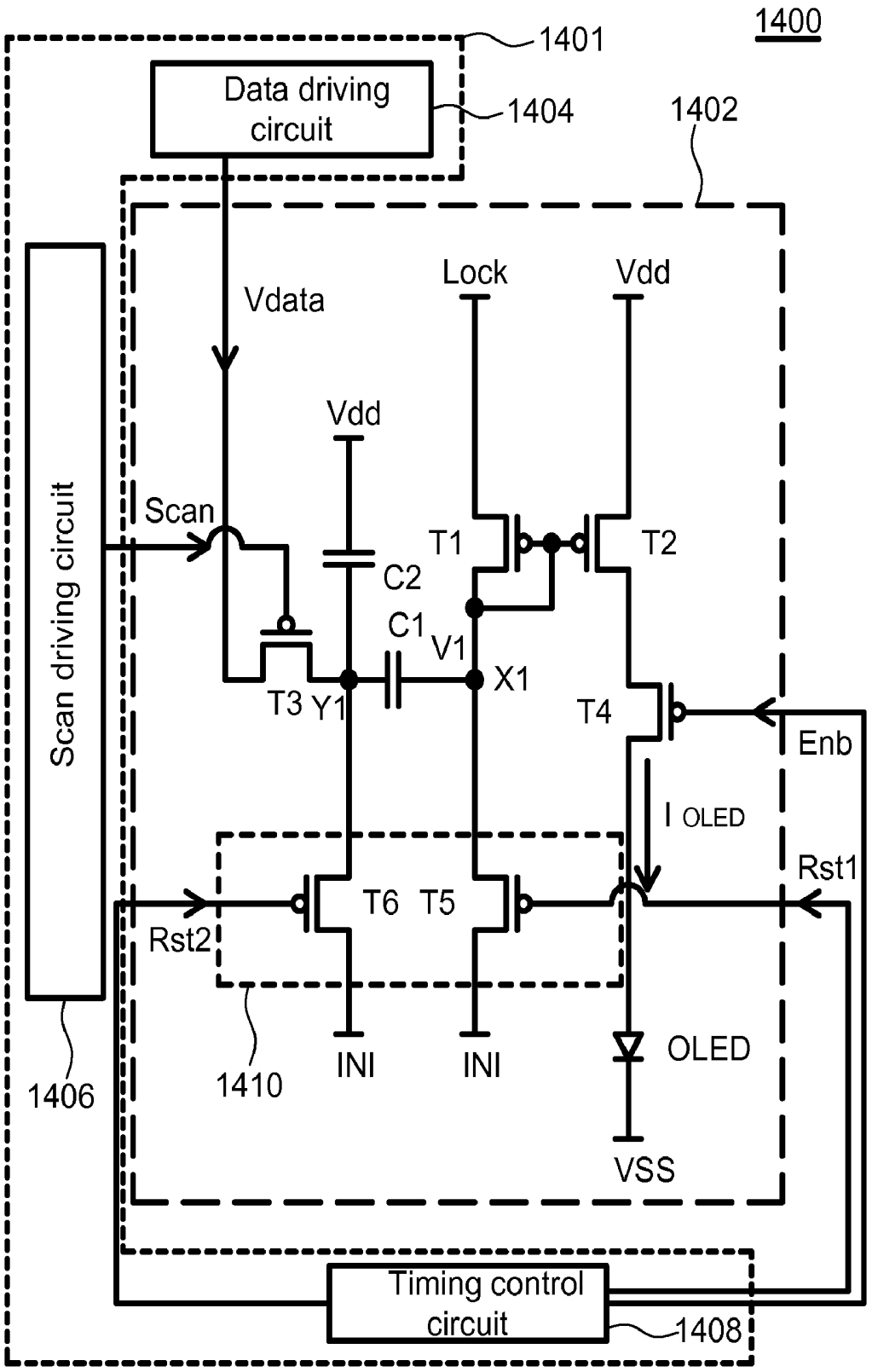

1400
1401
Data driving circuit
1404
1402
Vdata
Lock
Vdd
Vdd
Scan
Scan driving circuit
T1
T2
C2
C1
V1
X1
T3
Y1
T4
Enb
I OLED
Rst1
T6
T5
Rst2
INI
INI
OLED
VSS
1406
1410
Timing control circuit
1408

FIG. 14

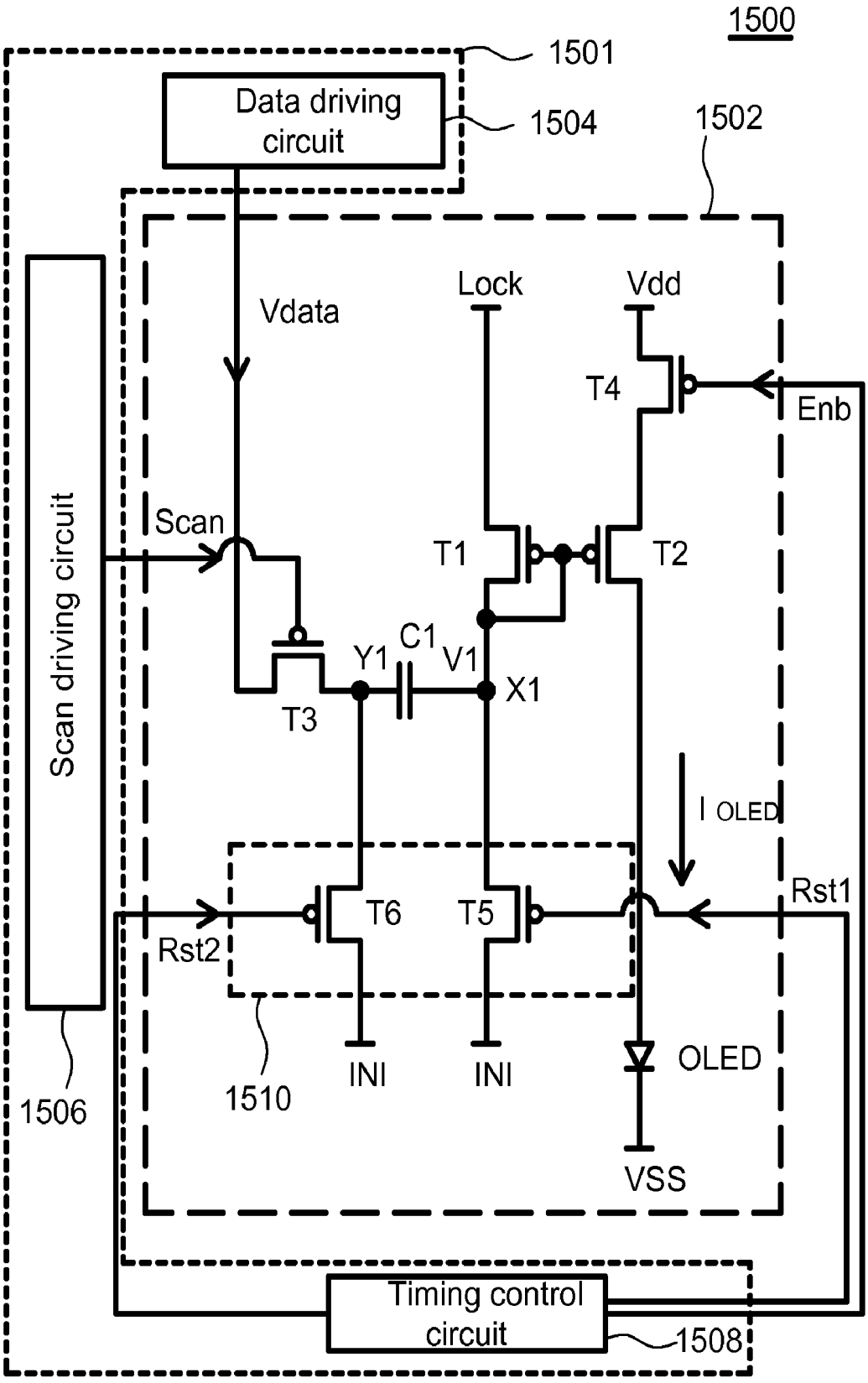

1500
1501
Data driving circuit
1504
1502
Vdata
Lock
Vdd
T4
Enb
Scan
T1
T2
Scan driving circuit
C1
Y1
V1
X1
T3
I OLED
Rst1
T6
T5
Rst2
INI
INI
OLED
1506
1510
VSS
Timing control circuit
1508

FIG. 15

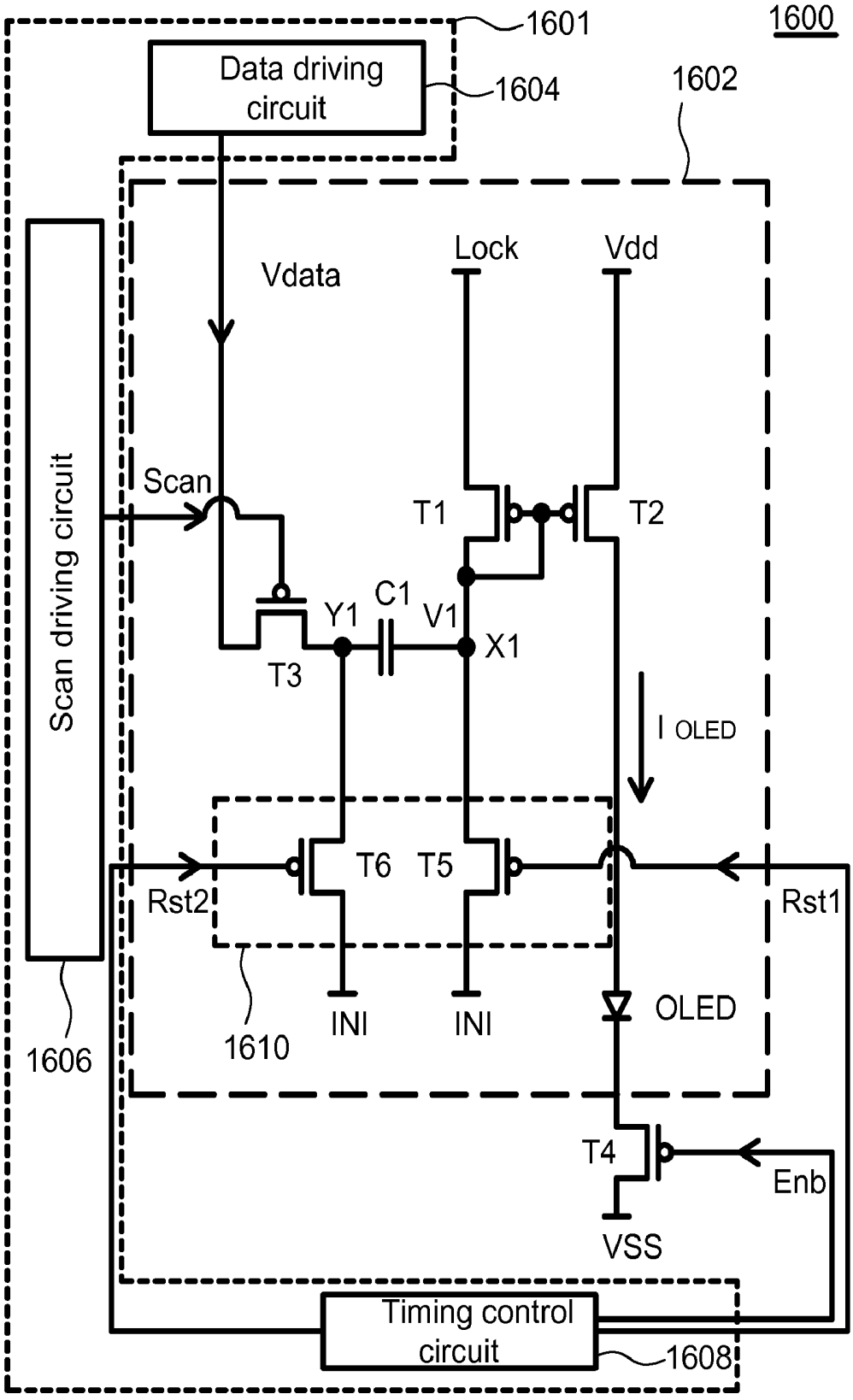

1600
1601
Data driving circuit
1604
1602
Vdata
Lock
Vdd
Scan
T1
T2
C1
Y1
V1
X1
T3
I OLED
Scan driving circuit
T6
T5
Rst2
Rst1
INI
INI
OLED
1606
1610
T4
Enb
VSS
Timing control circuit
1608

FIG. 16

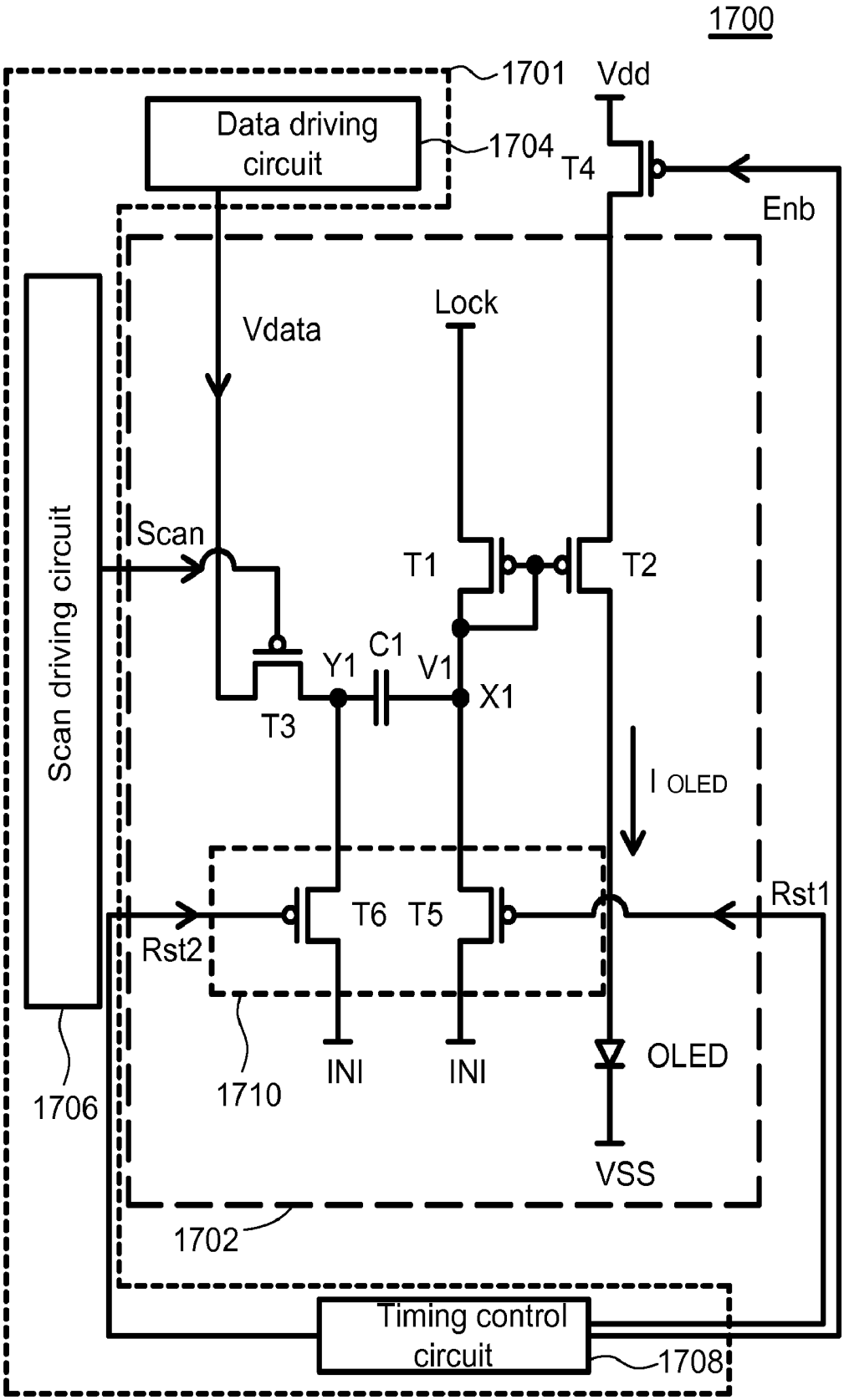

1700
1701
Vdd
Data driving circuit
1704
T4
Enb
Vdata
Lock
Scan driving circuit
Scan
T1
T2
Y1
C1
V1
X1
T3
I OLED
Rst1
T6
T5
Rst2
INI
INI
OLED
1706
1710
VSS
1702
Timing control circuit
1708

FIG. 17

ORGANIC LIGHT EMITTING DISPLAY HAVING ORGANIC LIGHT EMITTING DIODE CIRCUIT WITH VOLTAGE COMPENSATION AND TECHNIQUE THEREOF

[0001] This application claims the benefit of Taiwan application Serial No. 94143429, filed Dec. 8, 2005, the subject matter of which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The invention relates in general to an organic light emitting display, and more particularly to an organic light emitting diode circuit for such a display.

[0004] 2. Description of the Related Art

[0005] An organic light emitting diode circuit used in organic light emitting display normally stores signals for controlling the luminance of an organic light emitting diode (OLED) via thin film transistors (TFTs) and capacitors. However, the above TFTs, after prolonged use, will exhibit a threshold voltage (Vth) shift. This shift amount is related to the operation time of the TFTs and the current flowing therethrough.

[0006] In a display process, owing that the TFT for driving an OLED for each diode has a different current when turned on, and the driving TFTs will have different shift amounts of threshold voltage. As a result, the luminance of each diode will not have the same correspondence relation as the received pixel data, which in turn results in an uneven frame display.

[0007] In order to solve the above issue, a voltage compensation technique is applied to a conventional organic light emitting diode. Referring to FIG. **1**, a circuit diagram of a conventional organic light emitting diode is shown. An organic light emitting diode circuit **100** includes TFTs MP**1**~MP**5**, a storage capacitor Cst and an organic light emitting diode (OLED). The TFT MP**3** is controlled by a scan signal Scan and the TFT MP**1** is coupled between the TFT MP**3** and the storage capacitor Cst. The TFT MP**2** drives the OLED to illuminate according to a voltage of the storage capacitor Cst when the TFT MP**4** is turned on. The TFT MP**5** is controlled by a reset signal Rst and the TFT MP**4** is controlled by an enable signal Enb.

[0008] The conventional organic light emitting diode circuit **100**, as written pixel data Vdata, uses the TFT MP**1** with the same device feature as the TFT MP**2** to cancel the threshold voltage Vth**2** of the TFT MP**2**. More specifically, when the scan signal Scan is enabled, the TFT MP**3** is turned on and the pixel data Vdata charges the storage capacitor Cst via the TFTs MP**3** and MP**1**. In the meanwhile, due to a voltage compensation feature of the TFT MP**1**, the voltage level at point X, that is, a gate voltage of the TFT MP**2**, is lower than a voltage level at point Y, that is, a threshold voltage Vth**1** of the TFT MP**1**, and thus the voltage difference between the source and gate of the TFT MP**2** is increased by Vth**1**. The threshold voltage Vth**1** is substantially the same as the threshold voltage Vth**2**, and the voltage difference between the source and gate of the TFT MP**2** is just equal to difference between Vdd and the pixel voltage Vdata. Therefore, the current OLED flowing by the OLED is precisely related to the pixel voltage Vdata.

[0009] In the above compensation technique, the compensation operation is performed during a data writing stage to eliminate errors generated from the threshold voltage Vth**2**. However, recent OLED panels tend to be developed in high resolution and large size. As a result, the time for writing data is greatly reduced. However, the TFT MP**1** has small current as it is turned on, and thus it needs longer compensation time, which will result in an irregular operation of the TFT MP**1** and disability of the compensation mechanism. However, with the circuit design of a conventional voltage compensation arrangement, it is essential that the nodes X and Y both have a stable voltage state during the "data writing" stage, otherwise, a charge sharing issue will be generated at the frame display stage. Accordingly, the conventional voltage compensation arrangement is apt to exhibit the drawback that the the node X does not reach a stable voltage state for canceling Vth**2** due to inadequate time. In this situation, the TFT MP**1** is still turned on. As a result, the charge sharing issue is generated and the display luminance can not reach the predicted luminance in correspondence with the pixel voltage Vdata.

SUMMARY OF THE INVENTION

[0010] The invention is directed to an organic light emitting display and diode with a voltage compensation arrangement which improves the speed of threshold voltage compensation.

[0011] According to the present invention, an organic light emitting diode of an organic light emitting display equipped with a voltage compensation arrangement The organic light emitting diode circuit comprises a first capacitor, a first TFT, a second TFT, a third TFT, a reset circuit and an OLED. The first TFT has a first terminal for receiving a first reference voltage, and a second terminal coupled to its gate and a first end of the first capacitor. The second TFT has a first terminal for receiving a second reference voltage and a gate coupled to the gate of the first TFT. The third TFT has a first terminal for receiving a pixel voltage, a second terminal coupled to a second end of the first capacitor and a gate for receiving a scan signal. The reset circuit is for setting the first end of the first capacitor to have a first voltage level. The OLED has an anode coupled to a second terminal of the second TFT and a cathode for receiving a third reference voltage. The first voltage level is smaller than a voltage level of the first reference voltage.

[0012] The invention will become apparent from the following detailed description of the preferred but non-limiting embodiments. The following description is made with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. **1** is a circuit diagram of a conventional organic light emitting diode circuit.

[0014] FIG. **2** is a schematic diagram of an organic light emitting display according to a first embodiment of the invention.

[0015] FIG. **3** is a timing diagram of the organic light emitting diode circuit according to the first embodiment of the invention.

[0016] FIG. **4** is another example of the reset circuit depicted in FIG. **2**.

[0017] FIG. **5** is a further example of the reset circuit depicted in FIG. **2**.

[0018] FIG. **6** is an internal circuit diagram of the organic light emitting diode circuit with a second storage capacitor according to the first embodiment of the invention.

[0019] FIG. **7** is another example of the fifth TFT depicted in FIG. **2**.

[0020] FIG. **8** is a further example of the fifth TFT depicted in FIG. **2**.

[0021] FIG. **9** is yet another example of the fifth TFT depicted in FIG. **2**.

[0022] FIG. **10** is an internal circuit diagram of the organic light emitting diode circuit equipped with a voltage compensation arrnagement.

[0023] FIG. **11** is a timing diagram of the organic light emitting diode circuit according to a second embodiment of the invention.

[0024] FIG. **12** is another example of the reset circuit depicted in FIG. **10**.

[0025] FIG. **13** is another example of the reset circuit depicted in FIG. **10**.

[0026] FIG. **14** is an internal circuit diagram of the organic light emitting diode circuit with a second storage capacitor according to the second embodiment of the invention.

[0027] FIG. **15** is another example of the fifth TFT depicted in FIG. **10**.

[0028] FIG. **16** is a further example of the fifth TFT depicted in FIG. **10**.

[0029] FIG. **17** is yet another example of the fifth TFT depicted in FIG. **10**.

DETAILED DESCRIPTION OF THE INVENTION

[0030] The invention is directed to an organic light emitting display having a voltage compensation arrangement which improves the speed of threshold voltage compensation.

Embodiment One

[0031] FIG. **2** is a schematic diagram of an organic light emitting display according to a first embodiment of the invention. An organic light emitting display **200** includes a driving unit **201** and an organic light emitting diode circuit **202**. The driving unit **201** is for driving the organic light emitting diode circuit **202** and includes a data driving circuit **204**, scan driving circuit **206** and timing control circuit **208**. The data driving circuit **204** outputs a fifth voltage to the organic light emitting diode circuit **202** according to image data, wherein the fifth voltage is a pixel voltage Vdata or a low voltage Preset. The scan driving circuit **206** is for outputting a scan signal Scan. The timing control circuit **208** is configured to output a first control signal Enb to a fifth TFT T**5** and a second control signal Rst to a reset circuit **210**. The driving unit **201** also supplies a first voltage Lock, second voltage Vdd, third voltage Vss and fourth voltage INI. The organic light emitting diode circuit **202** includes a first capacitor C**1**, first TFT T**1**, second TFT T**2**, third TFT T**3**, fourth TFT T**4**, reset circuit **210** and an OLED. The TFTs T**1**~T**4** are exemplified to be p-typed metal oxide semiconductor (PMOS) transistors as shown in FIG. **2**.

[0032] The third TFT T**3** has a first terminal for receiving the pixel voltage Vdata or the low voltage Preset, a second terminal coupled to a second end of the first capacitor C**1** (i.e. the node Y**1** denoted in FIG. **2**) and a gate for receiving the scan signal Scan. The first TFT T**1** has a first terminal for receiving the first voltage Lock, and a second terminal and a gate coupled together to a first end of the first capacitor C**1** (i.e. the node X**1** denoted in FIG. **2**). The second TFT T**2** has a first terminal for receiving the second voltage Vdd and a gate coupled to the gate of the first TFT T**1**. The fourth TFT T**4** has a first terminal coupled to a second terminal of the second TFT T**2**, a second terminal coupled to an anode of the OLED and a gate for receiving the first control signal Enb.

[0033] A cathode of the OLED receives the third voltage Vss. The reset circuit **210**, which is formed by the fifth TFT T**5**, is for setting the first end (i.e. the node X**1**) of the first capacitor C**1** to have the first voltage level V**1**. The fifth TFT, such as a PMOS transistor, has a first terminal coupled to the first end X**1** of the first capacitor C**1**, a second terminal for receiving the fourth voltage INI and a gate for receiving the second control signal Rst. It should be noted that the above first voltage level V**1** is smaller than a voltage level of the first voltage Lock.

[0034] Referring to FIG. **3**, a timing diagram of the organic light emitting diode circuit according to the first embodiment of the invention is shown. In the 0-th stage 0 Stage (for displaying a previous frame), the scan signal Scan is set to have a voltage level such that the third TFT T**3** is turned off, the second control signal Rst is set to have a voltage level such that the fifth TFT T**5** is turned off, and the first control signal Enb is set to have a voltage level such that the fourth TFT T**4** is turned on. Therefore, the voltage at the node Y**1** is a pixel voltage Vdata' of the previous frame and the voltage at the node X**1** is a voltage X' of the previous frame. The voltage X' of the node X**1** is larger than the first voltage Lock. The first voltage Lock turns off the first TFT T**1** in the meanwhile the voltage X' turns on the second TFT T**2** to generate a current I_{OLED}. The current I_{OLED} is equal to $Kp*(Vsg-Vtp2)^2$. The voltage Vsg is voltage difference between the gate and source of the second TFT T**2**, which is (Vdd−X'). The voltage Vtp**2** is a threshold voltage of the third TFT T**2**. The current I_{OLED} drives the OLED to illuminate through the fourth TFT T**4**.

[0035] Following this, in the first stage (I Stage), the voltage level of the second control signal is set such that the fifth TFT T**5** is turned on, the voltage level of the scan signal Scan is set such that the third TFT T**3** is turned on and the voltage level of the first control signal Enb is set such that the fourth TFT T**4** is turned off. At this time, the data driving circuit **204** supplies a low voltage Preset. The low voltage Preset sets the voltage of the node Y**1** to be the predetermined low voltage Preset, such as −1V~0V through the turned-on third TFT T**3**. The voltage of the node X**1** is the fourth voltage INI due to turning on of the fifth TFT T**5**. At this stage, the first capacitor C**1** is reset by the low voltage Preset and the fourth voltage INI.

[0036] In the second stage II Stage, the voltage level of the second control signal is set such that the fifth TFT T**5** is

turned off while the scan signal Scan and the first control signal Enb remain to have the same voltage level as in the previous stage. Therefore, the third TFT T3 remains turned on and the fourth TFT T4 remains turned off. At this time, the voltage of the node Y1 is still the low voltage Preset and the voltage of the node X1 rises up to a second voltage level V2 due to the effect of the turned-off fifth TFT T5 and the first TFT T1. The second voltage level V2 is the first voltage Lock subtracted by the threshold voltage Vtp1 of the first TFT T1.

[0037] In the third stage (III Stage) i.e. a data writing stage, the voltage level of the control signal Enb is changed such that the fourth TFT T4 is turned on, the second control signal Rst and scan signal Scan remain to have the same voltage level as in the second stage. At this time, the data driving circuit **204** outputs the pixel voltage Vdata. The voltage Vdata is provided through the third TFT T3 to set the voltage of the node Y1 as the pixel voltage Vdata. The voltage of the node X1 also rises up to (Lock−Vtp1+Vdata−Preset) due to an effect of the first capacitor C1, which causes the first TFT T1 to be turned off. At the time, the voltage difference between the gate and source of the second TFT T2 is the second voltage Vdd subtracted by the voltage level of the node X1, i.e. Vdd−(Lock−Vtp1+Vdata−Preset). A feature at this stage lies in due to the turned-on fourth TFT T4, a conductive current I_{OLED} is generated corresponding to the voltage difference Vsg between the gate and source of the second TFT T2. The conductive current $I_{OLED}=Kp*(Vsg-Vtp2)^2$. The voltage difference Vsg is Vdd−(Lock−Vtp1+Vdata−Preset). Therefore, the current $I_{OLED}=Kp*(Vdd-(Lock-Vtp1+Vdata-Preset)-Vtp2)^2$. Owing to Vtp1 being approximately equal to Vtp2, the current I_{OLED} can be approximated to be $Kp*(Vdd-Lock-Vdata+Preset)^2$. The OLED thus has a luminance corresponding to the current I_{OLED}.

[0038] In the fourth stage (IV Stage) for displaying the present frame, except that the voltage level of the scan signal Scan is changed such that the third TFT T3 is turned off and no pixel voltage is inputted to the third TFT T3, other components have the same operation and the nodes have the same as in the third stage III Stage.

[0039] As mentioned above, in the second stage (II Stage), the organic light emitting diode circuit **202** has completed a compensation operation for the threshold voltage Vtp2. This helps prevent the TFT in charge of a compensation operation for a threshold voltage, i.e. the TFT MP1 in FIG. **1** having a lower speed of compensation mechanism and thus solves the charge sharing issue in the data writing stage due to unstable voltage compensation, which results in an error data voltage and frame luminance, in the prior-art arrangement. On the other hand, by controlling the first voltage Lock, the operational speed of the compensation mechanism can be also increased to reduce compensation time. Owing to this fewer components are used in this embodiment and thus renders it more applicable to a small-size panel, such as in a hand-held equipment.

[0040] In addition, the above reset circuit **210** can be also implemented in a different circuit structure. As shown in FIG. **4**, another reset circuit **210'** consists of a fifth TFT T5 wherein the fifth TFT T5 has a first terminal coupled to the first end (i.e. the node X1) of the first capacitor C1, and a second terminal and a gate coupled together for receiving the second control signal Rst. Alternatively, as shown in FIG. **5**, another reset circuit **210"** also consists of the fifth TFT T5, but is such that it has a first terminal coupled to the first end (i.e. the node X1) of the first capacitor C1, a second terminal coupled to the other end of the first capacitor C1 and a gate for receiving the second control signal Rst.

[0041] The organic light emitting diode circuit **202** can also be coupled to a second capacitor C2. As shown in FIG. **6**, in the organic light emitting diode circuit **202**, the second capacitor C2 has a first end coupled to the node Y1 and a second end for receiving the second voltage Vdd. The second capacitor C2 helps maintain a stable voltage difference between the nodes X1 and Y1.

[0042] Moreover, the above fourth TFT T4 is for controlling the current I_{OLED} to flow toward the OLED. Except for the disposition position as shown in FIG. **2**, the fourth TFT T4 can be also disposed at a position as shown in FIG. **7**. FIG. **7** is a schematic diagram of the second example of the organic light emitting display in the embodiment. In the organic light emitting diode circuit **702**, the fourth TFT T4 can also be disposed between the second voltage Vdd and the second TFT T2. That is, the fourth TFT T4 has a first terminal for receiving the second voltage Vdd, a second terminal coupled to the first terminal (a source) of the second TFT T2 and a gate for receiving the first control signal Enb.

[0043] Alternatively the fourth TFT T4 can also be coupled outside the organic light emitting diode circuit for controlling the current I_{OLED} to flow toward the OLED. As shown in FIG. **8**, which is a schematic diagram of the third example of the organic light emitting display in the embodiment, the fourth TFT T4 is coupled outside the organic light emitting diode circuit **802**. That is, the fourth TFT T4 has a first terminal coupled to a cathode of the OLED, a second terminal coupled to the third voltage Vss and a gate for receiving the first control signal Enb.

[0044] The fourth TFT T4 can also be coupled outside the organic light emitting diode circuit and between the second voltage Vdd and second TFT T2. As shown in FIG. **9**, which is a schematic diagram of the fourth example of the organic light emitting display of the first embodiment, the fourth TFT T4 is coupled outside the organic light emitting diode circuit **902** and has a first terminal coupled to the first terminal of the second TFT T2, a second terminal coupled to the first voltage Vdd and a gate for receiving the first control signal Enb.

Embodiment Two

[0045] The difference this embodiment and the first embodiment lies in the structure of the reset circuit. In this embodiment, the reset circuit consists of two TFTs which are respectively coupled to two ends of the first capacitor for resetting the first capacitor and setting a potential of the node X1.

[0046] Referring to FIG. **10**, a schematic diagram of an organic light emitting display according to a second embodiment of the invention is shown. An organic light emitting display **1000** includes a driving unit **1001** and an organic light emitting diode circuit **1002**. The driving unit **1001** includes a data driving circuit **1004**, scan driving circuit **1006** and timing controller **1008**. The organic light emitting diode circuit **1002** also includes a first capacitor C1, a first

TFT T1, a second TFT T2, a third TFT T3, a fourth TFT T4, a reset circuit **1010** and an OLED. The TFTs T1~T4 are exemplified as PMOS transistors as shown in FIG. **10**. The organic light emitting display **1000** has the same structure as that in the first embodiment. Thus, details thereof are omitted for brevity.

[0047] It should be noted that the reset circuit **1010** consists of a fifth TFT T5 and sixth TFT T6. The fifth TFT T5 and a sixth TFT T6 are PMOS transistors by way of example only. The fifth TFT T5 has a first terminal coupled to a first end (i.e. the node X1) of the first capacitor C1, the second terminal for receiving the fourth voltage INI and a gate for receiving the second control signal Rst1. The sixth TFT T6 has a first terminal coupled to a second end (i.e. the node Y1) of the first capacitor C1, a second terminal for receiving the fourth voltage INI and a gate for receiving the third control signal Rst2. The first voltage level V1 is smaller than a voltage level of the first voltage Lock.

[0048] Referring to FIG. **11**, a timing diagram of the organic light emitting diode circuit according to the second embodiment of the invention is shown. In the 0-th stage (0 Stage'), the voltage level of the scan signal Scan is set such that the third TFT T3 is turned off, the voltage levels of the second control signal Rst1 and third control signal Rst2 are set such that the fifth TFT T5 and sixth TFT T6 are both turned off. Therefore, the voltage of the node Y1 is the pixel voltage Vdata' of the previous frame and the voltage of the node X1 is the voltage X' of the previous frame. The voltage X' of the node X1 is larger than the first voltage Lock and thus the first TFT T1 is turned off in the meanwhile the voltage X' also turns on the second TFT T2 to generate the current I_{OLED}. The current I_{OLED} is $Kp*(Vdd-Y'-Vtp2)^2$. The voltage Vsg is voltage difference between the gate and source of the second TFT T2, which is Vdd−Y'. The voltage Vtp2 is a threshold voltage of the second TFT T2. The current I_{OLED} drives the OLED to illuminate through the fourth TFT T4.

[0049] Following this, in the first stage (I Stage'), the voltage level of the scan signal Scan is changed such that the third TFT T3 is turned off, the voltage levels of the second control signal Rst1 and the third control signal Rst2 are changed such that the fifth TFT T5 and sixth TFT T6 are both turned on. At the time, the voltage of the nodes X1 and Y1 is the fourth voltage INI, such as −2V~−1V. At this stage, the first capacitor C1 is reset through the fourth voltage INI.

[0050] In the second stage (II Stage'), the voltage level of the second control signal is changed such that the fifth TFT T5 is turned off while the scan signal Scan, the first control signal Enb and the third control signal Rst2 remain at the same voltage level as in the first stage (I Stage'). Therefore, at this time, the voltage of the node Y1 is still INI and the voltage of the node X1 rises up to a second voltage level V2 due to an effect of the turned-off fifth TFT T5 and the first TFT T1. The second voltage level V2 is the first voltage Lock subtracted by the threshold voltage Vtp1 of the first TFT T1. In other words, this stage is for setting the second end Y1 of the first capacitor C1 to have the voltage level Lock−Vtp1.

[0051] In the third stage (III Stage) i.e. a data writing stage, the voltage level of the first control signal Enb is changed such that the fourth TFT T4 is turned on, the voltage level of the third control signal Rst2 is changed such that the sixth TFT T6 is turned off, the voltage level of the scan signal Scan is changed such that the third TFT T3 is turned on and the second control signal Rst1 remains at the original voltage level. At this time, the data driving circuit **1004** outputs the pixel voltage Vdata. The pixel voltage Vdata is provided through the turned-on third TFT T3 to set the voltage of the node Y1 as the pixel voltage Vdata. The voltage of the node X1 also rises up to (Lock−Vtp1+Vdata−INI) due to an effect of the first capacitor C1, which causes the first TFT T1 to be turned off. At this time, the voltage difference Vsg between the gate and source of the second TFT T2 is the second voltage Vdd subtracted by the voltage level of the node X1, i.e.

$$Vdd-(Lock-Vtp1+Vdata-INI).$$

$Vsg-Vtp=Vdd-(Lock-Vtp+Vdata-INI)-Vtp=Vdd-Lock-Vdata+INI$. Therefore, the current $I_{OLED}=Kp*(Vdd-(Lock-Vtp1+Vdata-INI)-Vtp2)^2$. Owing to the fact that Vtp1 is approximately equal to Vtp2, the current I_{OLED} can be approximated to be $Kp*(Vdd-Lock-Vdata+INI)^2$. The OLED therefore has a luminance corresponding to the current I_{OLED}.

[0052] In the fourth stage (IV Stage') i.e. the frame display stage, except that the voltage level of the scan signal Scan is changed such that the third TFT T3 is turned off and no pixel voltage is inputted to the third TFT T3, other components exhibit the same operation and the nodes have the same as in the third stage (III Stage').

[0053] As mentioned above, it can known that in the second stage (II Stage'), the organic light emitting diode circuit **1002** has completed a compensation operation for the threshold voltage Vtp2. This helps prevent the TFT in charge of a compensation operation for a threshold voltage, i.e. the TFT MP1 in FIG. **1** having a lower speed of compensation mechanism and thus solve the charge sharing issue in the data writing stage due to unstable voltage compensation, which results in an error data voltage and frame luminance, in the prior-art technique. On the other hand, by controlling the first voltage Lock, the operational speed of the compensation mechanism can be also increased to reduce compensation time. Owing to the fact that more components are used, this embodiment tends to be more applicable to large-size panels, such as in a display equipment.

[0054] Besides, the above reset circuit **1010** can be also implemented using different circuit structure. As shown in FIG. **12**, another example of a reset circuit **1010'** consists of the fifth TFT T5 and sixth TFT T6, wherein the fifth TFT T5 has a first terminal coupled to the first end (i.e. the node X1) of the first capacitor C1, and a second terminal for receiving the fourth voltage INI, and a gate for receiving the second control signal Rst1. The sixth TFT T6 has a gate for receiving the third control signal Rst2. Or as shown in FIG. **13**, another reset circuit **1010"** is also consisted of the fifth TFT T5 and sixth TFT T6, but the fifth TFT T5 has a first terminal coupled to the first end (i.e. the node X1) of the first capacitor C1, and a second terminal and a gate coupled together for receiving the second control signal Rst1. The sixth TFT T6 has a first terminal coupled to the second end (i.e. the node Y1) of the first capacitor C1, a second terminal coupled and a gate together for receiving the third control signal Rst2.

[0055] The organic light emitting diode circuit **1002** can also be coupled to a second capacitor C2. As shown in FIG.

14, in the organic light emitting diode circuit **1402**, the second capacitor C**2** has a first end coupled to the node Y**1** and a second end for receiving the second voltage Vdd. The second capacitor C**2** helps maintain a stable voltage difference between the nodes X**1** and Y**1**.

[**0056**] Moreover, the above fourth TFT T**4** is for controlling the current I_{OLED} to flow toward the OLED. Except for the disposition position shown in FIG. **10**, the fourth TFT T**4** can be also disposed at a position as shown in FIG. **15**. FIG. **15** is a schematic diagram of the second example of the organic light emitting display in the embodiment. In the organic light emitting diode circuit **1502**, the fourth TFT T**4** has a first terminal for receiving the second voltage Vdd, a second terminal coupled to the first terminal of the second TFT T**2** and a gate for receiving the first control signal Enb.

[**0057**] Alternatively, the fourth TFT T**4** can also be coupled outside the organic light emitting diode circuit for controlling the current IOLED to flow toward the OLED. As shown in FIG. **16**, which is a schematic diagram of the third example of the organic light emitting display in the embodiment, the fourth TFT T**4** is coupled outside the organic light emitting diode circuit **1602**. The fourth TFT T**4** has a first terminal coupled to a cathode of the OLED, a second terminal coupled to the third voltage Vss and a gate for receiving the first control signal Enb.

[**0058**] The fourth TFT T**4** can also be coupled outside the organic light emitting diode circuit and between the second voltage Vdd and second TFT T**2**. As shown in FIG. **17**, which is a schematic diagram of the fourth example of the organic light emitting display in the embodiment, the fourth TFT T**4** is coupled outside the organic light emitting diode circuit **1702** and has a first terminal coupled to the first terminal of the second TFT T**2**, a second terminal coupled to the first voltage Vdd and a gate for receiving the first control signal Enb.

[**0059**] The organic light emitting display and the organic light emitting diode circuit with the voltage compensation technique disclosed in connection with the above embodiments of the invention can increase the speed of the compensation process and consequently eliminate the drawback of uneven frame display of an active matrix organic light emitting display (AMOLED) due to the present low-temperature poly-silicone technique.

[**0060**] While the invention has been described by way of example and in terms of a different embodiments, it is to be understood that the invention is not limited thereto. On the contrary, the scope of the present invention is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

What is claimed is:

1. A method for driving an organic light emitting diode circuit, the organic light emitting diode circuit comprising a first capacitor, a first thin film transistor (TFT), a second TFT and an organic light emitting diode (OLED), a first end of the first capacitor coupled to a gate of the second TFT, a first terminal of the first TFT receiving a first voltage, a second terminal of the first TFT coupled to a gate of the first TFT and the first end of the first capacitor, a first terminal of the second TFT receiving a second voltage, a second terminal of the second TFT outputting a pixel current to an anode of the OLED, a cathode of the OLED receiving a third voltage, the method comprising:

turning off the OLED;

supplying a fourth voltage to the first end of the first capacitor and a fifth voltage to a second end of the first capacitor in duration when the OLED is turned off such that voltage difference of the fourth voltage and the first voltage is large enough for turning on the first TFT; and

removing the fourth voltage such that the first end of the first capacitor has a first voltage level due to an effect of the second TFT in duration when the organic TFT is turned off and the second end of the first capacitor remains at the fifth voltage;

supplying a pixel voltage to the second end of the first capacitor in duration when the OLED is turned off and the first end of the first capacitor has the first voltage level; and

turning on the OLED to output the pixel current to the OLED via the third TFT according to a voltage level of the first end of the first capacitor.

2. The method according to claim 1, wherein the step of providing the fifth voltage is performed via a data driving circuit and a third TFT, a first terminal of the third TFT receives the fifth voltage outputted by the data driving circuit, a second terminal of the third TFT is coupled to the second end of the first capacitor, a gate of the third TFT is for receiving a scan signal and when the scan signal has a voltage level capable of turning on the third TFT, the third TFT supplies the fifth voltage to the second end of the first capacitor.

3. The method according to claim 1, wherein the step of turning off the OLED is implemented by a fourth TFT, a first terminal and a second terminal of the fourth TFT are coupled in series to a path of the pixel current, the first terminal is a source or drain, and the second terminal is a drain or source.

4. The method according to claim 1, wherein the voltage level of the fifth voltage is substantially the same as the voltage level of the fourth voltage.

5. An organic light emitting diode circuit, comprising:

a first capacitor;

a first TFT, having a first terminal for receiving a first voltage and a second terminal and a gate coupled together to a first end of the first capacitor;

a second TFT, having a first terminal for receiving a second voltage and a gate coupled to the gate of the first TFT;

a third TFT, having a first terminal for receiving a pixel voltage, a second terminal coupled to a second end of the first capacitor and a gate for receiving a scan signal;

a reset circuit, for setting the first end of the first capacitor to have a first voltage level; and

an OLED, having an anode coupled to a second terminal of the second TFT and a cathode for receiving a third voltage;

wherein the first voltage level is smaller than a voltage level of the first voltage.

6. The organic light emitting diode circuit according to claim 5, further comprising:

a fourth TFT, having a first terminal coupled to the second terminal of the second TFT, a second terminal coupled to the anode of the OLED and a gate for receiving a first control signal.

7. The organic light emitting diode circuit according to claim 5, further comprising:

a fourth TFT, having a first terminal for receiving the second voltage, a second terminal coupled to the first terminal of the second TFT and a gate for receiving a first control signal.

8. The organic light emitting diode circuit according to claim 5, wherein the reset circuit is used for resetting the first capacitor, and the reset circuit comprises:

a fifth TFT, having a first terminal coupled to the first end of the first capacitor, a second terminal for receiving a fourth voltage and a gate for receiving a second control signal.

9. The organic light emitting diode circuit according to claim 5, wherein the reset circuit is used for resetting the first capacitor, and the reset circuit comprises:

a fifth TFT, having a first terminal coupled to the first end of the first capacitor, and a second terminal and a gate coupled to each other for receiving a second control signal.

10. The organic light emitting diode circuit according to claim 5, wherein the reset circuit is used for resetting the first capacitor, and the reset circuit comprises:

a fifth TFT, having a first terminal coupled to the first end of the first capacitor, a second terminal coupled to the second end of the first capacitor and a gate for receiving a second control signal.

11. The organic light emitting diode circuit according to claim 5, further comprising:

a second capacitor, having a first end coupled to the second end of the first capacitor and a second end for receiving the second voltage.

12. The organic light emitting diode circuit according to claim 5, wherein the reset circuit is used for resetting the first capacitor and the reset circuit comprises:

a fifth TFT, having a first terminal coupled to the first end of the first capacitor, a second terminal for receiving a fourth voltage and a gate for receiving a second control signal;

a sixth TFT, having a first terminal coupled to the second end of the first capacitor, a second terminal for receiving the fourth voltage and a gate for receiving a third control signal.

13. The organic light emitting diode circuit according to claim 5, wherein the reset circuit is used for resetting the first capacitor and the reset circuit comprises:

a fifth TFT, having a first terminal coupled to the first end of the first capacitor, a second terminal for receiving a fourth voltage and a gate for receiving a second control signal;

a sixth TFT, having a first terminal coupled to the second end of the first capacitor, a second terminal coupled to the second terminal of the fourth TFT and a gate for receiving a third control signal.

14. The organic light emitting diode circuit according to claim 5, wherein the reset circuit is used for resetting the first capacitor and the reset circuit comprises:

a fifth TFT, having a first terminal coupled to the first end of the first capacitor, and a second terminal and a gate coupled to each other for receiving a second control voltage;

a sixth TFT, having a first terminal coupled to the second end of the first capacitor, and a second terminal and a gate coupled to each other for receiving a third control signal.

15. An organic light emitting display, comprising:

at least an organic light emitting diode circuit, comprising:

a first capacitor;

a first TFT, having a first terminal for receiving a first voltage and a second terminal coupled to a gate of the first TFT and a first end of the first capacitor;

a second TFT, having a first terminal for receiving a second voltage and a gate coupled to a gate of the first TFT;

a third TFT, having a first terminal for receiving a pixel voltage, a second terminal coupled to a second end of the first capacitor and a gate for receiving a scan signal;

a reset circuit, for setting the first end of the first capacitor to have a first voltage level; and

an OLED, having an anode coupled to a second terminal of the second TFT and a cathode for receiving a third voltage; and

a driving unit, for driving the organic light emitting diode circuit, the driving unit comprising:

a data driving circuit, for outputting the pixel voltage;

a scan driving circuit, for outputting the scan signal; and

a timing control circuit, for controlling the reset circuit to set the first end of the first capacitor to have the first voltage level;

wherein the first voltage level is smaller than a voltage level of the first voltage and the driving unit is for supplying the first voltage, the second voltage and the third voltage.

16. The organic light emitting display according to claim 15, wherein the organic light emitting diode circuit further comprises:

a fourth TFT, having a first terminal coupled to the second terminal of the second TFT, a second terminal coupled to the anode of the OLED and a gate for receiving a first control signal outputted by the timing control circuit.

17. The organic light emitting display according to claim 15, wherein the organic light emitting diode circuit further comprises:

a fourth TFT, having a first terminal for receiving the second voltage, a second terminal coupled to the first

terminal of the second TFT and a gate for receiving a first control signal outputted by the timing control circuit.

18. The organic light emitting display according to claim 15, wherein the reset circuit is used for resetting the first capacitor, and the reset circuit comprises:

a fifth TFT, having a first terminal coupled to the first end of the first capacitor, a second terminal for receiving a fourth voltage provided by the driving unit and a gate for receiving a second control signal outputted by the timing control circuit.

19. The organic light emitting display according to claim 15, wherein the reset circuit is used for resetting the first capacitor, and the reset circuit comprises:

a fifth TFT, having a first terminal coupled to the first end of the first capacitor, and a second terminal and a gate coupled to each other for receiving a second control signal outputted by the timing control circuit.

20. The organic light emitting display according to claim 15, wherein the reset circuit is used for resetting the first capacitor, and the reset circuit comprises:

a fifth TFT, having a first terminal coupled to the first end of the first capacitor, a second terminal coupled to the second end of the first capacitor and a gate for receiving a second control signal outputted by the timing control circuit.

21. The organic light emitting display according to claim 15, further comprising:

a second capacitor, having a first end coupled to the second end of the first capacitor and a second end for receiving the second voltage.

22. The organic light emitting display according to claim 15, wherein the reset circuit is used for resetting the first capacitor and the reset circuit comprises:

a fifth TFT, having a first terminal coupled to the first end of the first capacitor, a second terminal for receiving a fourth voltage provided by the driving unit and a gate for receiving a second control signal outputted by the timing control circuit; and

a sixth TFT, having a first terminal coupled to the second end of the first capacitor, a second terminal for receiving the fourth voltage and a gate for receiving a third control signal outputted by the timing control circuit.

23. The organic light emitting display according to claim 15, wherein the reset circuit is used for resetting the first capacitor and the reset circuit comprises:

a fifth TFT, having a first terminal coupled to the first end of the first capacitor, a second terminal for receiving a fourth voltage provided by the driving unit and a gate for receiving a second control signal outputted by the timing control circuit; and

a sixth TFT, having a first terminal coupled to the second end of the first capacitor, a second terminal coupled to the second terminal of the fourth TFT and a gate for receiving a third control signal outputted by the timing control circuit.

24. The organic light emitting display according to claim 15, wherein the reset circuit is used for resetting the first capacitor and the reset circuit comprises:

a fifth TFT, having a first terminal coupled to the first end of the first capacitor, and a second terminal and a gate coupled to each other for receiving a second control voltage outputted by the timing control circuit; and

a sixth TFT, having a first terminal coupled to the second end of the first capacitor, and a second terminal and a gate coupled to each other for receiving a third control signal outputted by the timing control circuit.

* * * * *

专利名称(译)	具有电压补偿的有机发光二极管电路的有机发光显示器及其技术		
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摘要(译)

具有电压补偿技术的有机发光显示器的有机发光二极管电路包括第一电容器，第一TFT，第二TFT，第三TFT，复位电路和OLED。第一TFT具有用于接收第一电压的第一端子，以及耦合到其栅极和第一电容器的第一端的第二端子。第二TFT具有用于接收第二参考电压的第一端子和耦合到第一TFT的栅极的栅极。第三TFT耦合到第一电容器并接收像素电压和扫描信号。复位电路将第一电容器的第一端设置为具有第一电压电平。 OLED具有耦合到第二TFT的第二端子的阳极和用于接收第三参考电压的阴极。第一电压电平小于第一参考电压的电压电平。